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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,576	07/29/2002	Jung-An Wang	9445-US-PA	3242

31561 7590 11/30/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
AMIN, NIRAV S	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,576	WANG ET AL.	
	Examiner	Art Unit	
	Nirav S Amin	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/13/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al (US Patent No. 6,006,327) herein after referred to as Chang.

Chang teachs the claimed invention, comprising:

a datapath chipset [220];

a power-supply/memory-clearing selecting circuit for switching between a power-supply status and a memory-clearing status for the peripheral configuration memory [circuitry for receiving user input for setting the options for the motherboard, col. 4, lines 57 - 62, col. 5, lines 5 - 8];

a latching circuit [latch 281, fig. 2, col. 4, line 66 - col. 5, line 1], electrically coupled to and in between the power-supply/memory-clearing selecting circuit and the datapath chipset for providing a clearing latch signal when the power-supply status is switched to the memory-clearing status [col. 5, lines 50 - 57].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Goodwin in view of Chang et al (US Patent No. 6,006,327) herein after referred to as Chang.

Goodwin discloses:

a computer main board (100) used within a computer:

a peripheral configuration memory (106) for storing an effective peripheral configuration value [Column 4, lines 32-33];

a power-supply/memory-clearing selecting circuit (104) capable of switching between a power-supply status and a memory clearing status for the peripheral configuration memory;

Goodwin does not expressly disclose:

a datapath chipset having a peripheral configuration memory for storing an effective peripheral configuration value,

and a latching circuit, electrically coupled to and in between the power-supply/memory-clearing selecting circuit and the datapath chipset for providing a clearing latch signal when the power-supply status is switched to the memory-clearing status.

Chang discloses:

a chipset (220) for storing an effective peripheral configuration value [Column 4, lines 47-49] and

a latching circuit (281) electrically coupled to the chipset for allowing the user to set options to the motherboard [Column 4, lines 56-58].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a chipset and a latching circuit as taught by Chang in the motherboard taught by Goodwin for the benefit of allowing the user to set options to the motherboard [Column 4, lines 56-58].

Claim 17-20 rejected under 35 U.S.C. 102(b) as being anticipated by Goodwin et al (US Patent No. 6,473,856) herein after referred to as Goodwin.

Goodwin discloses:

a peripheral configuration memory clearing method [Figure 5], adapted to clear the content of a peripheral configuration memory of a computer main board [Column 6, lines 28-30],

the computer main board being capable of providing a clearing latch signal that indicates whether a user has previously set a clearing of the peripheral configuration memory [Column 6, lines 24-27], the method comprising:

reading the clearing latch signal [Column 6, lines 26-28], writing a clearing value into the peripheral configuration memory when the clearing latch signal is set and [Column 6, lines 27-31],

resetting the clearing latch signal [Column 6, lines 31-32].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav S Amin whose telephone number is (571) 272-3821. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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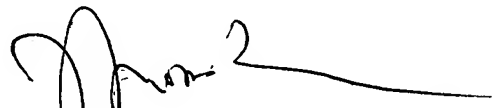

THOMAS LEE
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